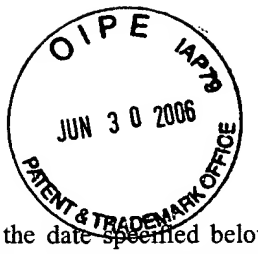

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June 26, 2006 — Denise Sheridan

Date — Denise Sheridan

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	: 09/654,115	Confirmation No.	: 5616
Applicant	: Dean A. Klein	Examiner	: Tuan A. Vu
Filed	: August 30, 2000	Attorney Docket No.	
Art Unit	: 2193	Customer No.	: 27,076
Title	: SYSTEM AND METHOD FOR DETERMINING THE CACHEABILITY OF CODE AT THE TIME OF COMPILING		

REPLY BRIEF TRANSMITTAL

Mail Stop Appeal Brief –Patents
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P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Transmitted herewith, in duplicate, is the Appellant's Reply Brief to the Examiner's Answer dated May 10, 2006.

Respectfully submitted,
DORSEY & WHITNEY LLP

Edward W. Bulchis
Registration No. 26,847

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APPELLANT'S REPLY BRIEF (37 C.F.R. § 41.41)

Sir:

This Reply Brief is in response to the Examiner's Answer dated May 10, 2006. Applicant will selectively address some of the Examiner's arguments in the following sections to the extent applicant understands these arguments.

I. CLAIMED MEMORY DEVICE PHYSICALLY SEPARATE FROM CLAIMED CACHE

The Examiner initially contends that the claims do not specify that the memory device containing the program code is physically separate from the cache, and, therefore, separate pages of the same memory devices can correspond to the claimed "memory device containing a program code" and the claimed "cache." This contention is inconsistent with any reasonable interpretation of the language of the claims. For example, claim 25 specifies that a processor "direct[s] selected portions of the program code to a cache...." If, as the Examiner contends, the memory containing the program code was simply a page of the memory that was

separate from the page of the memory constituting the cache, then the claim would require that the program code in the memory be directed to itself, which is a nonsensical interpretation. As another example, claim 1 specifies "bus circuitry, operatively connecting the processor, the cache circuitry, and the main memory." If, as the Examiner contends, the cache circuitry and the main memory could be the same physical device, there would be no bus connecting them to each other and to the processor.

II. PROGRAM CODE STORED IN MEMORY DEVICE DIRECTED TO CACHE

The Examiner also ignores the requirement in claim 1 and 25 that the program code stored in the memory device is selectively transferred to the cache. If, for purposes of argument, applicant agreed with the Examiner that the claimed memory device corresponds to Mattson's "static cache" and the claimed cache corresponds to Mattson's "dynamic cache" (or vice versa) then for the Mattson patent alone or in combination to anticipate claim 25 or render obvious claim 1, it would be necessary for the patent to describe program code stored in the static cache being directed to the dynamic cache (or vice versa). However, Mattson does not describe the information stored in one cache as ever being transferred to the other cache. Instead, instructions are transferred from another device to one cache or the other depending upon their branching behavior. In contrast, claims 1 and 25 specify that selected portions of the information or program code stored in the memory device are directed to the cache. Thus, even under the Examiner's interpretation of Mattson's teachings, Mattson, taken alone or in combination, cannot render claim 1 obvious or anticipate claim 25.

Finally, the Examiner cites Holler for teaching the concept of storing instructions in memory. Regardless of the propriety of basing an anticipation rejection on Holler in combination with Mattson, Holler still fails to disclose directing instructions stored in a memory device to a cache based on cacheability determinations. While Figure 1 of the Holler patent does show a memory 13 and a cache 12, the patent does not state that the memory 13 stores code. Nor does the Holler patent state that anything stored in the memory 13 is ever transferred to the cache 12. In fact, the patent mentions the word "memory" only in line 59 of column 2, and thus never describes what is stored in the memory 13 or to where whatever is stored in the memory 13 is ever transferred. Therefore, it certainly does not disclose that information or program code

stored in the memory 13 is directed to the cache 12 based on cacheability determinations made during compilation. Besides, the Examiner has already taken the position that different pages of Mattson's memory device constitute the static and dynamic caches. Therefore, it is not apparent how the teaching of Holler could be combined with the teachings of Mattson consistent with that interpretation. Presumably Mattson's memory device would be substituted for Holler's memory 13. But different pages of that memory device would still constitute the claimed cache, so there would be no teaching of code being transferred from a memory device to a cache based on cacheability determinations made during compilation.

III. MOTIVATION TO COMBINE REFERENCES

In attempting to provide some rationale for combining references, the Examiner has ignored the fact the Mattson and Morrison teach two fundamentally different techniques for solving the branch prediction problem. Mattson teaches storing instructions in different pages of memory based on their branching performance. Morrison teaches re-ordering the instructions based on their branching performance. One skilled in the art admittedly might use the teachings of either reference to solve the branch prediction problem. But no reason has been given why one would use the combined teachings of both patents to solve the problem since there would be no advantage to simultaneously using both techniques.

Respectfully submitted,
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